A1

100, allowing data and/or commands to be transferred between the components. --

Paragraph beginning at page 3, line 19 has been amended as follows:

A2

-- FIG. 3 shows a signal routing configuration that reduces the area required for each signal line 200 running between the MCU 120 and the memory unit. In this configuration, the signal line 200 has a width of approximately 18 mils with a 5 mil neck down portion 205 contacting the corresponding pin 155 on the memory unit. The signal line 210 exiting the pin 155 also has a width of approximately 18 mils with a 5 mil neck down portion 215 contacting the pin 155. The two neck down portions 205, 215 run substantially parallel to each other for a distance, and then at an acute angle for another distance, the portions are separated by a gap 220. This gap 220 also has a width of approximately 5 mils. The neck down portions 205, 215 are not separated by a ground trace. --

Paragraph beginning at page 5, line 1 has been amended as follows:

A3

-- FIG. 4 shows the neck down portions 205, of the signal line 200, and neck down portion 215 of signal line 210, on a multi-layer circuit board 225. The neck down portions 205, 215 into and out of the memory unit are formed on a single layer of the circuit board 225 and are separated by a gap 220 in which no traces are formed. No ground trace lies between the neck down